# Workshop 03 - Sequential Hardware

### Workshop 3 - Sequential Hardware

**Make sure you are marked off during this session. Only when the marker is ready to enter your marks, flag yourself in the pracmarker:**

[**https://cs.adelaide.edu.au/services/pracmarker/**](https://cs.adelaide.edu.au/services/pracmarker/)

**As a backup. As you are developing your answers make sure that you update the logbook associated with this workshop.**

This workshop is worth 0.83% of your course mark.  These marks will be given for your participation in your session. As with the first session the purpose of this session is to give you the chance to work with the design of hardware. In this case building simple components from basic gates that you saw in chapter 1.

In this workshop you will be producing HDL code.  For the HDL you may find t[he HDL Survival Guide (Links to an external site.)Links to an external site.](http://www.nand2tetris.org/software/HDL%20Survival%20Guide.html) useful.

The questions below are derived from the third chapter of the nand2tetris book and project 03 of the Nand2teris course. See [this link (Links to an external site.)Links to an external site.](http://nand2tetris.org/03.php) for more information and test scripts.

Answer the following questions.

##### Question 1 (elementary)

Purely combinatorial circuits don't need a clock. However, a clock becomes important once we have a memory to store data. Briefly describe why a clock is important for memory to function properly. (Hint: this relates to the definition of memory itself).

##### Question 2 (elementary)

Read chapter 3.1 of the textbook - under the paragraph heading "Time Matters". In the Hack machine only memory chips and registers have sequential logic. This means that the other (combinatorial) logic is time insensitive. This means that, depending on the length of the wires, operations such as those in the ALU will, for some moments of time, be producing garbage as they wait for all signals coming in to be in sync.

Explain why this period of garbage is not of consequence to the correct working of the chip.

##### Question 3 (more challenging)

Build and test using HDL  a one-bit register from project 3 of the Nand2Tetris course ([http://www.nand2tetris.org/03.php (Links to an external site.)Links to an external site.](http://www.nand2tetris.org/03.php)).

**Write brief notes**  logging your development process for this one bit gate.

##### Question 4 (more challenging)

Build and test using HDL a 16 bit register from project 03 of the Nand2Tetris course.

**Include notes** logging your development process for this 16bit register.

At the end of your session go to the [pracmarker system](https://cs.adelaide.edu.au/services/pracmarker) (navigate to workshop 3 of this course)  and, when the supervisor is ready to check your work, flag your work for marking.

#### Additional Questions

##### Question 5 - Clocks

What would happen in the architecture below if memory could update without waiting for the clock? Hint: think about the relative speeds of operations.

##### RAM Chip

Draw an implementation for a RAM chip consisting of two words of memory. The interface for this chip is shown below:

##### End of Questions